classmate

Date

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DATA LOGICS AND MICRO-PROCESSORS

M

2^3 2^2 2^1 2^0
8 4 2 1

Excess 3-codes

Q. Convert $(15)_{10}$ in excess-3 code.

$$\begin{array}{cc} 1 & 5 \\ +3 & +3 \\ \hline 4 & 8 \\ \downarrow & \downarrow \\ 0100 & 1000 \end{array}$$

$\therefore (15)_{10} = (01001000)_2$

Q. Convert $(231.75)_{10}$ to excess-3 code.

$$\begin{array}{ccccc} 2 & 3 & 1 & . & 7 & 5 \\ +3 & +3 & +3 & & +3 & +3 \\ \hline 5 & 6 & 4 & & 10 & 8 \\ \downarrow & \downarrow & \downarrow & & \downarrow & \downarrow \\ 0101 & 0110 & 0100 & . & 1010 & 1000 \end{array}$$

$\therefore (231.75)_{10} = (010101100100.10101000)$

Q. Reverse: 1100 1010 0011. 0111 0101

$$\begin{array}{cccccc} 1100 & 1010 & 0011 & . & 0111 & 0101 \\ \downarrow & \downarrow & \downarrow & & \downarrow & \downarrow \\ 12 & 10 & 3 & & 7 & 5 \\ -3 & -3 & -3 & & -3 & -3 \\ \hline 9 & 7 & 0 & . & 4 & 2 \end{array}$$

$(110010100011.01110101)_2 = (970.42)_{10}$

SUMMARY.

- → 3 exess codes & reverse
- → gray code & reverse
- → all gates
- → by using NAND and NOR gates...
- → SOP
- → POS
- → K-Map
- → Half adder
- → full adder

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Turning to hexadecimal...

16	970	10
16	60	12
16	3	3
	0	

$\rightarrow (3\,(12)\,(10))_{16} = (3CA)_{16}$

$.42 \rightarrow (.6B851E)$

.42
×16
6.72
(6) 11.52
(11) 8.32
(8) 5.12
(5) 1.92
(1) 14.72
(14) 11.52

$\therefore (970.42)_{10} = (3CA.6B851E)_{16}$

Gray Codes

- this is to secure our data.
- these codes are implemented
- only one bit change in 2 successive numbers.
- reduce switching frequencies.
- Conversions
  1: Take MSB as it is
  2: Add MSB to the next bit
  3: Write the sum and ignore the carry
  4: Repeat.

Q. $(1011)_2 \longrightarrow$ gray code.

1 0 1 1

MSB +1 +0 +1

$$\boxed{1 \quad 1 \quad 1 \quad 0} \longrightarrow \text{gray code}$$

g_3 g_2 g_1 g_0

$A \oplus B = A\bar{B} + \bar{A}B = Y$

A	B	Y
0	0	
0	1	
1	0	
1	1	

when no of 1s odd ⇒ 1
other wise ⇒ 0
↓
a.k.a. odd 1's detector

b_3 b_2 b_1 b_0

1 0 1 1

MSB +1 +0 +1

↓ ↓ ↓ ↓

1 1 1 0

g_3 g_2 g_1 g_0

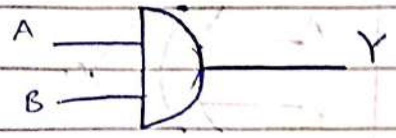
$g_3 = b_3$
$g_2 = b_3 \oplus$ b
$g_1 = b_2 \oplus$ b
$g_0 = b_1 \oplus$ b

Logic Gates

Acts as ~~a~~ building block for digital circuits.

AND Gate

- symbol:

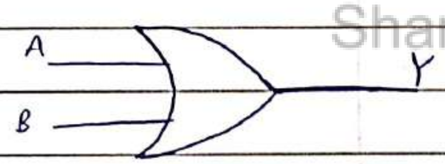


- truth table:

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

OR Gate

- symbol:

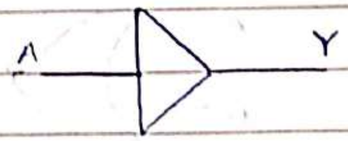


- truth table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

NOT Gate

- symbol:

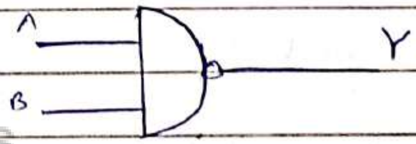


- truth table:

A	Y
0	1
1	0

NAND Gate

- symbol:

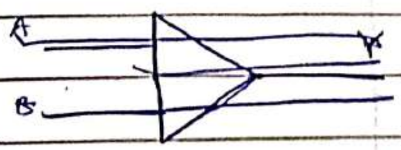


- truth table:

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

~~NOT Gate~~

- ~~symbol:~~



~~truth table:~~

~~A~~	~~B~~	~~Y~~
~~0~~	~~0~~	
~~0~~	~~1~~	
~~1~~	~~0~~	
~~1~~	~~1~~	

NOR Gate

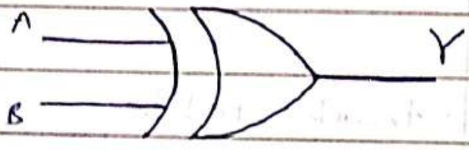
- symbol:

- truth table:

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

XOR Gate

- symbol:

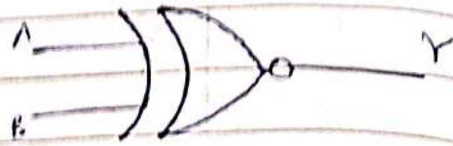


- truth table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

X-NOR Gate

- symbol:



- truth table:

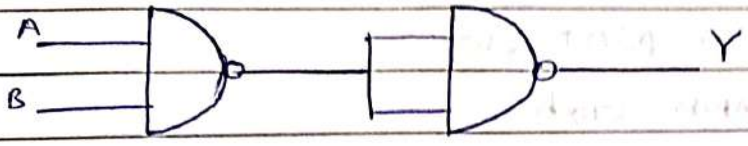
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Universal Gates

NAND and NOR gates are called universal as any digital circuit can be implemented by using these two gates.

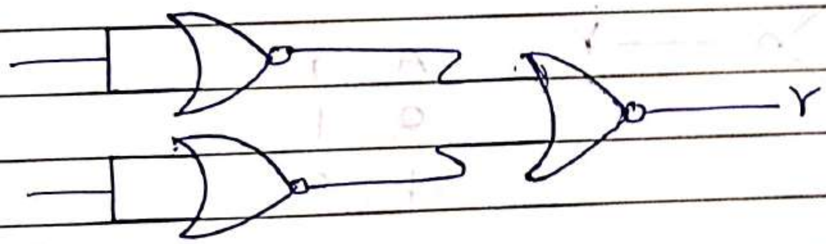
Implementation of AND Gates:

a) By using NAND Gates only



A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

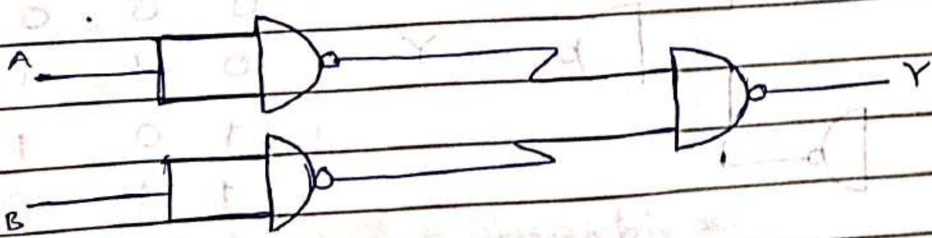
b) By using NOR Gates only



A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

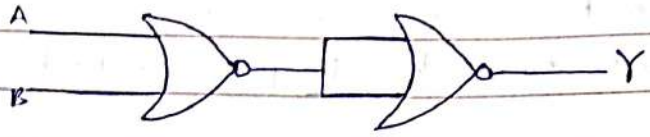
Implementation of OR Gate

a) By using NAND Gates only



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

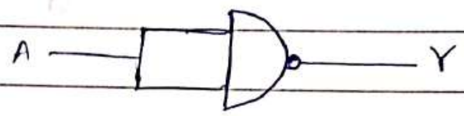
b) By using NOR Gates only



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Implementation of NOT Gates:

a) By using NAND Gate



A	Y
0	1
1	0

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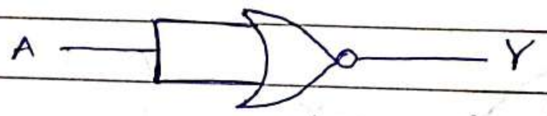
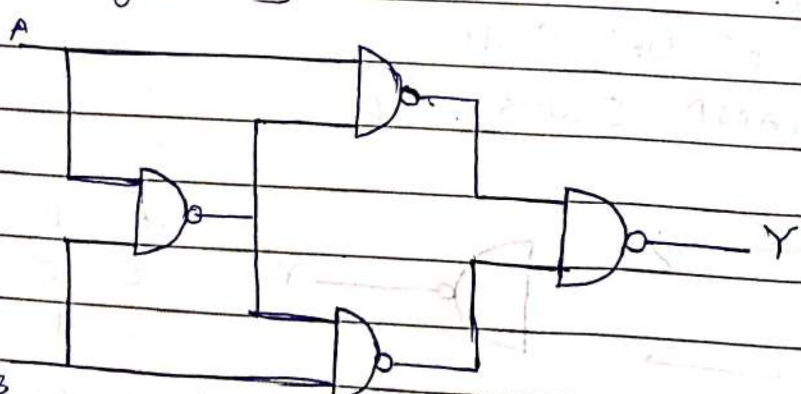
b) By using NOR Gate



A	Y
0	1
1	0

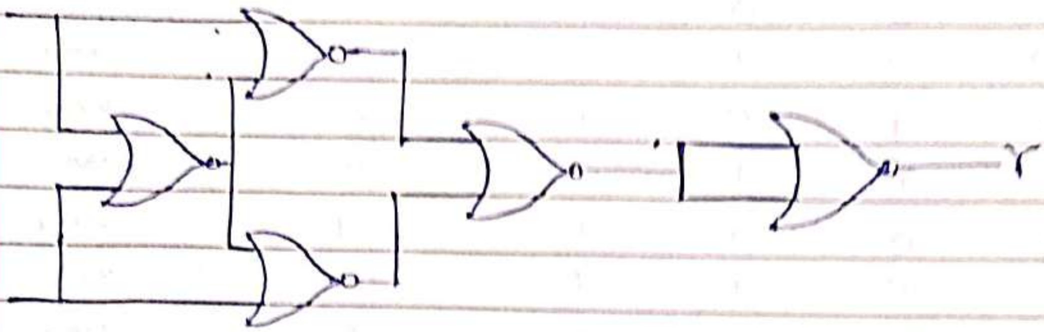
Implementation of XOR Gates:

a) By using NAND Gate



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

b) By using NOR Gate



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

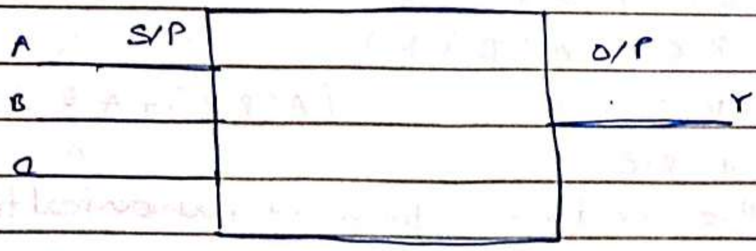
29/7/24 **Boolean func^n and representation**

Boolean func^n

SOP (Sum of products) — POS (Product of sums)

Sum of products (SOP):

$\bar{A} \cdot B \cdot \bar{C} + A \cdot \bar{B} \cdot C + A \cdot B \cdot C$



- total no. of combination $= 2^n$ where n = no. of variables

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(Example)

A	B	C	Y	Decimal	Min terms
0	0	0	0	0	m_0
0	0	1	0	1	m_1
0	1	0	1	2	m_2
0	1	1	0	3	m_3
1	0	0	1	4	m_4
1	0	1	1	5	m_5
1	1	0	1	6	m_6
1	1	1	1	7	m_7

- Standardized / Canonical form:

$$F(A,B,C) = \bar{A}\cdot B\cdot \bar{C} + A\cdot \bar{B}\cdot \bar{C} + A\cdot \bar{B}\cdot C + A\cdot B\cdot \bar{C} + A\cdot B\cdot C$$

→ consider only the high values of Y

→ write thier expressions. and add.

→ ~~Ex~~ in min. form:-

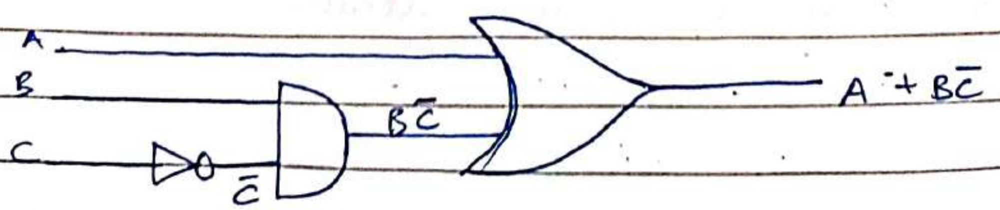
$$F(A,B,C) = m_2 + m_4 + m_5 + m_6 + m_7$$
$$= \sum_m (2,4,5,6,7)$$

. Non-canonical / minimal SOP form:

$$F(A,B,C) = \bar{A}\cdot B\cdot \bar{C} + A\cdot \bar{B}\cdot \bar{C} + A\cdot \bar{B}\cdot C + A\cdot B\cdot \bar{C} + A\cdot B\cdot C$$
$$= \bar{A}\cdot B\cdot \bar{C} + A\cdot \bar{B}\,(\bar{C}+C) + AB\,(\bar{C}+C)$$
$$= \bar{A}\cdot B\cdot \bar{C} + A\cdot \bar{B}\,(1) + AB(1)$$
$$= \bar{A}\cdot B\cdot \bar{C} + A\,(\bar{B}+B)$$
$$= \bar{A}\cdot B\cdot \bar{C} + A \qquad [\bar{A}(B\cdot\bar{C}) + A = A + B\cdot\bar{C}]$$
$$= A + B\cdot\bar{C}$$

→ this is the reduced form of canonical form.

→ representation



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Q. Simplify the expression:

$Y(A,B) = \sum_m (0, 2, 3)$

Ans combinations $= 2^2 = 4$

A	B	Y	min terms	Decimal
0	0	1	m_0	0
0	1	0	m_1	1
1	0	1	m_2	2
1	1	1	m_3	3

$F(A,B) = \bar{A}\cdot\bar{B} + A\cdot\bar{B} + A\cdot B$

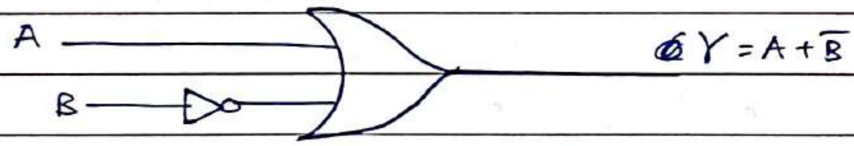
$= \bar{A}\cdot\bar{B} + A(\bar{B}+B)$

$= \bar{A}\cdot\bar{B} + A(1)$

$= A + \bar{B}$ $[\bar{A}X + A = A + X]$

$\therefore$ The simplified expression is $A+\bar{B}$.

Representation:



Q. For the given truth table, minimize the SOP operation.

A	B	Y	Decimal
0	0	0	0
0	1	1	1
1	0	0	2
1	1	1	3

Ans. $F(A,B) = \sum_m (1, 3)$

$= \bar{A}\cdot B + A\cdot B$

$= B(\bar{A}+A) = B$

Representation:

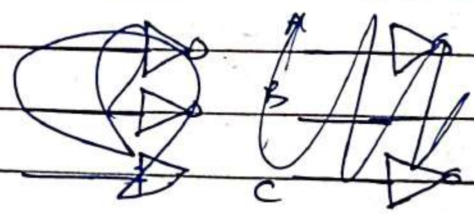
B ——————— Y

Q. $Y(A, B, C) = \sum_m (0, 2, 3, 6, 7)$

A	B	C	Y	min
0	0	0	1	m_0
0	0	1	0	m_1
0	1	0	1	m_2
0	1	1	1	m_3
1	0	0	0	m_4
1	0	1	0	m_5
1	1	0	1	m_6
1	1	1	1	m_7

$$F(A,B,C) = \bar{A}\cdot\bar{B}\cdot\bar{C} + \bar{A}\cdot B\cdot\bar{C} + \bar{A}\cdot B\cdot C + A\cdot B\cdot\bar{C} + A\cdot B\cdot C$$
$$= \bar{A}\cdot\bar{B}\cdot\bar{C} + \bar{A}\cdot B(\bar{C} + C) + A\cdot B(\bar{C} + C)$$
$$= \bar{A}\cdot\bar{B}\cdot\bar{C} + \bar{A}\cdot B + A\cdot B$$
$$= \bar{A}\cdot\bar{B}\cdot\bar{C} + B$$
$$= B + \bar{A}\cdot\bar{C}$$

Representation:



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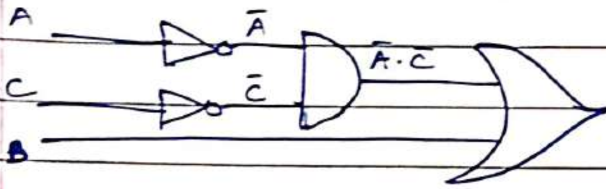
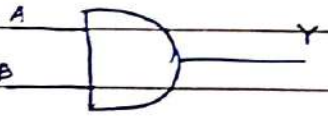


$Y = B + \bar{A}\cdot\bar{C}$

DLM Lab

AND

Symbol:

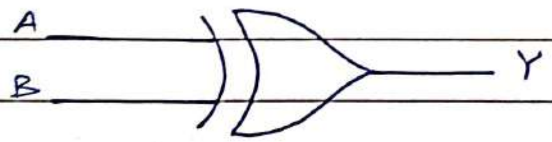


Truth table:

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

X-OR

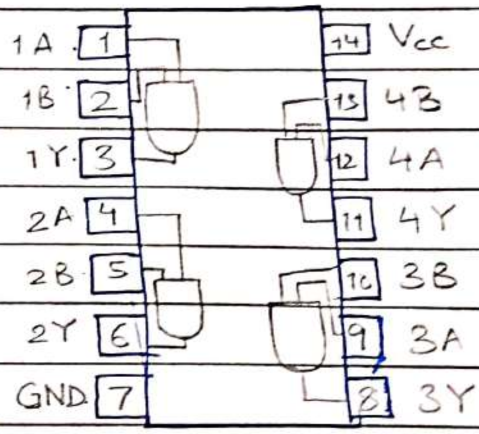
Symbol:



Truth table:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

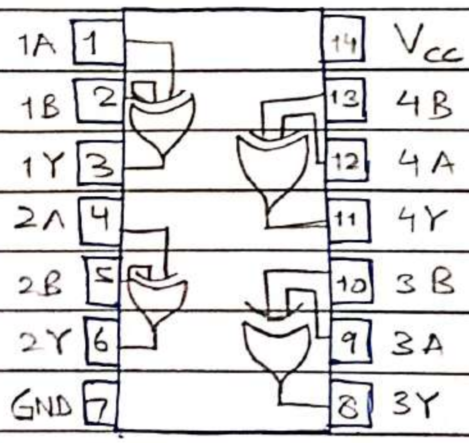
U74HC08L-01:



Funcⁿ table:

I/P(A)	I/P(B)	O/P
H	H	H
H	L	L
L	H	L
L	L	L

SN54HC86N:



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Solving one problem with SOP and POS

A	B	C	Y	m	SOP
1	1	1	1	m_0	A - 1
1	1	0	0	m_1	$\bar{A}$ - 0
1	0	1	1	m_2	
1	0	0	1	m_3	$Y(A,B,C) = \sum_m (0,2,3,6,7)$
0	1	1	0	m_4	
0	1	0	0	m_5	
0	0	1	1	m_6	
0	0	0	1	m_7	

$$Y(A,B,C) = \sum_m (0,2,3,6,7)$$

$$= (A \cdot B \cdot C) + (A \cdot \bar{B} \cdot C) + (A \cdot \bar{B} \cdot \bar{C}) + (\bar{A} \cdot \bar{B} \cdot C) + (\bar{A} \cdot \bar{B} \cdot \bar{C})$$

$$= AC(B+\bar{B}) + \bar{B} \cdot \bar{C}(A+\bar{A}) + \bar{A} \cdot \bar{B} \cdot C$$

$$= A \cdot C + \bar{B} \cdot \bar{C} + \bar{A} \cdot \bar{B} \cdot C$$

$$= \cancel{\bar{B} \cdot C + A} \quad AC + \bar{B}(C + \bar{A}C)$$

$$= \cancel{AC + \bar{B}(C+}$$

$$= A \cdot C + \bar{B}(\bar{C} + \bar{A} \cdot C)$$

$$= A \cdot C + \bar{B}(C + \bar{A})$$

$$= A \cdot C + \bar{B} \cdot C + \bar{B} \cdot \bar{A}$$

$=$

A	B	C	Y	m
0	0	0	1	m_0
0	0	1	0	m_1
0	1	0	1	m_2
0	1	1	1	m_3
1	0	0	0	m_4
1	0	1	0	m_5
1	1	0	1	m_6
1	1	1	1	m_7

SOP

$A = 1$

$\bar{A} = 0$

POS

$A = 0$

$\bar{A} = 1$

$$Y = \sum_m (0,2,3,6,7)$$
$$= m_0 + m_2 + m_3 + m_6 + m_7$$
$$= (\bar{A}\cdot\bar{B}\cdot\bar{C}) + (\bar{A}\cdot B\cdot\bar{C}) + (\bar{A}\cdot B\cdot C) + (A\cdot B\cdot\bar{C}) + (A\cdot B\cdot C)$$
$$= \bar{A}\cdot\bar{C}(\bar{B}+B) + A\cdot B(\bar{C}+C) + (\bar{A}\cdot B\cdot C)$$
$$= \bar{A}\cdot\bar{C} + A\cdot B + \bar{A}\cdot B\cdot C$$
$$= B(A+\bar{A}\cdot C) + \bar{A}\bar{C} \qquad \cancel{= \bar{A}(\bar{C}+B\cdot C) + A\cdot B}$$
$$= B(A+C) + \bar{A}\bar{C}$$
$$= B\cdot A + B\cdot C + \bar{A}\cdot\bar{C}$$

POS

$$Y = \prod M(1,4,5)$$
$$= (A\cdot\bar{B}\cdot\bar{C})\cdot(\bar{A}+\bar{B}+C)\cdot(\bar{A}\cdot\bar{B}\cdot\bar{C})$$
$$= (A+\bar{B}+\bar{C})\cdot(\bar{A}+\bar{B})\cdot(C\bar{C})$$
$$= (A+\bar{B}+\bar{C})\cdot(\bar{A}+\bar{B})+0$$
$$= \cancel{B+(A\bar{C}\cdot\bar{A})} \quad \bar{B} + (A+\bar{C})\cdot\bar{A}$$
$$= \bar{B} + (0) + (\bar{A}\cdot\bar{C})$$
$$= \bar{B} + \bar{A}\bar{C}$$

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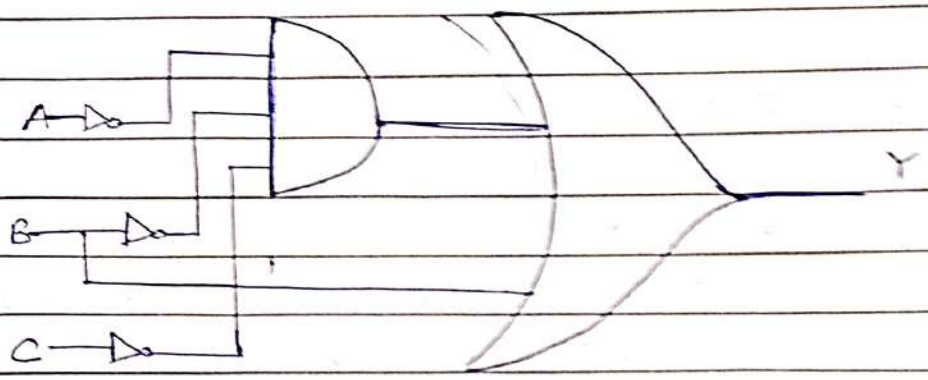
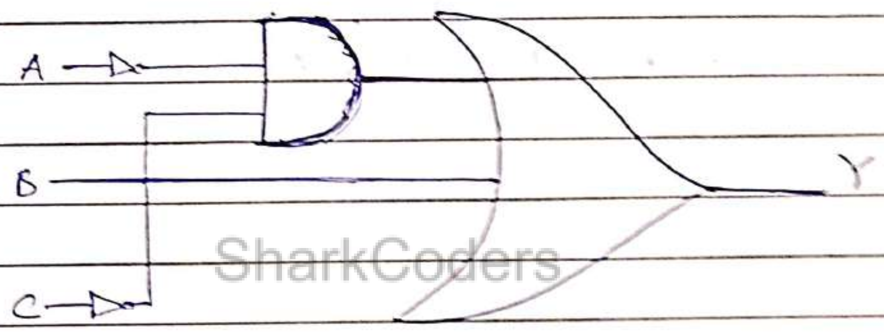
SOP - $Y = \bar{A}\bar{B}\bar{C} + B$



POS - $\bar{A}\cdot\bar{C} + B$



Q.

A	B	C	Y	m
0	0	0	0	m_0
0	0	1	1	m_1
0	1	0	1	m_2
0	1	1	1	m_3
1	0	0	0	m_4
1	0	1	1	m_5
1	1	0	0	m_6
1	1	1	1	m_7

$\cancel{Y(A,B,C) = \sum_m (0,2,3,6,7)}$

$\cancel{= (\bar{A}\cdot\bar{B}\cdot\bar{C}) + (\bar{A}\cdot B\cdot\bar{C}) + (\bar{A}\cdot B\cdot C) + (A\cdot B\cdot\bar{C}) + (A\cdot B\cdot C)}$

$\cancel{= \bar{A}\cdot\bar{C}(\bar{B}+B) +}$

$= \bar{A}\cdot B(\bar{C}\cdot C) + A\cdot B(\bar{C}+C) + (A\cdot\bar{B}\cdot\bar{C})$

$= \bar{A}\ \cancel{B + A\cdot B + \bar{A}\cdot\bar{B}}\cdot\bar{C}$

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~~$= B + \bar{A} \cdot \bar{B} \cdot \bar{C}$~~

POS

~~$A - 0 \quad \Pi M($~~

~~$\bar{A} - 1$~~

$Y = \sum_m (1, 2, 3, 5, 7)$

$= (\bar{A} \cdot \bar{B} \cdot C) + (\bar{A} \cdot B \cdot \bar{C}) + (\bar{A} \cdot B \cdot C) + (A \cdot \bar{B} \cdot C) + (A \cdot B \cdot C)$

~~$= \bar{A} \cdot B(\bar{C} + C) + A \cdot C(\bar{B} \cdot B) + (\bar{A} \cdot \bar{B} \cdot C)$~~

~~$= \bar{A} \cdot B + A \cdot C + (\bar{A} \cdot \bar{B} \cdot C)$~~

$= \bar{A} \cdot C(\bar{B} + B) + A \cdot C(\bar{B} \cdot B) + (\bar{A} \cdot B \cdot \bar{C})$

$= \bar{A} \cdot C + A \cdot C + \bar{A} \cdot B + \bar{C}$

$= C + \bar{A} \cdot B + \bar{C} \quad = C + \bar{A}B$

POS

$A - 0$

$A - 1$

$Y = \Pi M(0, 4, 6)$

$= M_0 + M_4 + M_6$

$= (A+B+C) \cdot (\bar{A}+B+C) \cdot (\bar{A}+\bar{B}+C)$

~~$(A+C) \cdot (B+$~~

$= (B+C) + (A\bar{A}) \cdot (\bar{A} + \bar{B} + C)$

$= (B+C) \cdot (\bar{A} + \bar{B} + C)$

$= (C) \cdot (B) + (\bar{A} + \bar{B})$

$= C + (B\bar{A}) + (B\bar{B})$

$= \bar{A}B + C$

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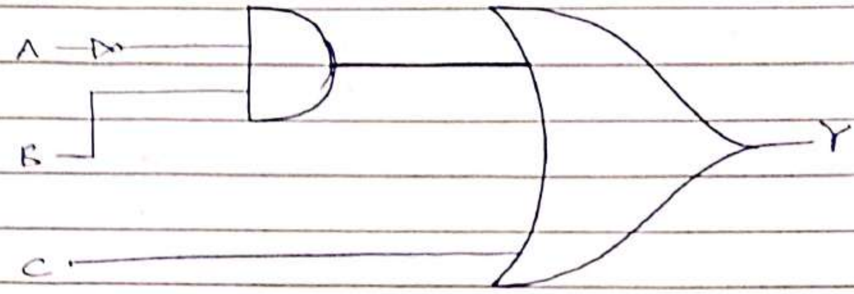
$Y = C + \bar{A}B$



$Y = \bar{A}B$

5/8/24 K-Map (Karnaugh Map)

Pictorial representation method that is used to minimize various boolean expressions without using the boolean algebra theorems along with the eq^n manipulations.

- can be a special version of the truth table
- can easily minimize various expressions that have two or four variables.

E.g.: $F(A,B,C) = Y$

$\boxed{\text{Works on gray codes}}$
(only one digit changes)

0	0
0	1
1	1
1	0

A \ BC	00	01	11	10
0	000 0	001 1	011 3	010 2
1	100 4	101 5	111 7	110 $\boxed{6}$

→ m terms

$2^2\ 2^1\ 2^0$

4 2 1

A	B	C	Y	m
0	0	0	0	m_0
0	0	1	0	m_1
0	1	0	1	m_2
0	1	1	0	m_3
1	0	0	1	m_4
1	0	1	1	m_5
1	1	0	1	m_6
1	1	1	0	m_7

SOP :- $[A - 1 ; \bar{A} - 0]$

$F(A,B,C) = \sum_m = (2, 4, 5, 6)$

$= (\bar{A}\cdot B\cdot\bar{C}) + (A\cdot\bar{B}\cdot\bar{C}) + (A\cdot\bar{B}\cdot C) + (A\cdot B\cdot\bar{C})$

$= \cancel{A\,\bar{C}\,(\bar{B}\,B) + (A\cdot\bar{B}\cdot C) + (\bar{A}\cdot B\cdot\bar{C})}$

$= B\bar{C}\,(\bar{A} + A) + (A\cdot\bar{B}\cdot\bar{C}) + (A\cdot\bar{B}\cdot C)$

$= B\bar{C} + (A\bar{B})(\bar{C} + C)$

$= B\bar{C} + A\bar{B}$

POS :- $[\bar{A} - 1 ; A - 0]$

$F(A,B,C) = \Pi M(0, 1, 3, 7)$

$\cancel{= (\bar{A}\cdot\bar{B}\cdot\bar{C}) + (\bar{A}\cdot\bar{B}\cdot C) + (\bar{A}\cdot B\cdot C) + (A\cdot B\cdot C)}$

$\cancel{= (\bar{A}\cdot\bar{B})(\bar{C} + C) + BC\,(\bar{A} + A)}$

$\cancel{= \bar{A}\cdot\bar{B} + BC}$

$= (\bar{A} + \bar{B} + \bar{C})\cdot(\bar{A} + \bar{B} + C)\cdot(\bar{A} + B + C)\cdot(A + B + C)$

$= \bar{A} + \bar{B} + (\bar{C}\cdot C) \cdot B + C + (\bar{A}\cdot A)$

$= (\bar{A} + \bar{B}) + 0 \cdot (B + C) + 0$

$= \cancel{\bar{A} + \bar{B} + B + C} \quad (\bar{A} + \bar{B})\cdot(B + C)$

$= \cancel{\bar{A} + C} \quad \bar{A}\cdot B + \bar{A}\cdot C + \bar{B}B + \bar{B}C$

$= \bar{A}\cdot B + \bar{A}\cdot C + \bar{B}C$

$= A\bar{B} + A\bar{C} + B\bar{C}$

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K - Map

A \ BC	00	01	11	10
0	0	0	0	1
1	1	1	0	1

$B\bar{C}$

$A\bar{B}$

$\therefore F(A,B,C) = Y = A\bar{B} + B\bar{C}$

POS :- $[\bar{A} - 1 ; A - 0]$

A	B	C	Y	m
0	0	0	0	m_0
0	0	1	0	m_1
0	1	0	1	m_2
0	1	1	0	m_3
1	0	0	1	m_4
1	0	1	1	m_5
1	1	0	1	m_6
1	1	1	0	m_7

POS :-

$F(A,B,C) = Y = \Pi M(0,1,3,7)$

$= (A+B+C)\cdot(A+B+\bar{C})\cdot(A+\bar{B}+\bar{C})\cdot(\bar{A}+\bar{B}+\bar{C})$

$= [(A+B)+(C\cdot\bar{C})]\cdot[(\bar{B}+\bar{C})+(A\cdot\bar{A})]$

$= (A+B) \cdot (\bar{B}+\bar{C})$

$= A\bar{B} + A\bar{C} + B\bar{B} + B\bar{C}$

$= A\bar{B} + A\bar{C} + B\bar{C}$

Q.

A	B	C	Y	m
0	0	0	1	m_0
0	0	1	0	m_1
0	1	0	1	m_2
0	1	1	1	m_3
1	0	0	0	m_4
1	0	1	0	m_5
1	1	0	1	m_6
1	1	1	1	m_7

K-Map :-

A \ BC	00	01	11	10
0	000: 1 (0)	001: 0 (1)	011: 1 (3)	010: 1 (2)
1	100: 0 (4)	101: 0 (5)	111: 1 (7)	110: 1 (6)

$\bar{A}\bar{C} + BC + B\bar{C} = F(A,B,C) = Y$

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A	B	C	Y	m
0	0	0	0	m_0
0	0	1	1	m_1
0	1	0	0	m_2
0	1	1	1	m_3
1	0	0	1	m_4
1	0	1	1	m_5
1	1	0	1	m_6
1	1	1	0	m_7

K-Map - (NEXT PAGE)

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A \ BC	00	01	11	10
0	0	1	1	0
1	1	1	0	1

$F(A, B, C) = Y = A\bar{B} + \bar{A}C + A.B.\bar{C}$

Q.

A	B	C	D	Y	m
0	0	0	0	0	m_0
0	0	0	1	0	m_1
0	0	1	0	0	m_2
0	0	1	1	1	m_3
0	1	0	0	0	m_4
0	1	0	1	0	m_5
0	1	1	0	1	m_6
0	1	1	1	1	m_7
1	0	0	0	1	m_8
1	0	0	1	1	m_9
1	0	1	0	0	m_{10}
1	0	1	1	0	m_{11}
1	1	0	0	0	m_{12}
1	1	0	1	0	m_{13}
1	1	1	0	1	m_{14}
1	1	1	1	0	m_{15}

AB \ CD	00	01	11	10
00			1	
01			1	1
11				1
10	1	1		

12/8/24 Half Adder

A combinational arithmetic circuit that adds two numbers and producebs a sum width and a carry width both at its output.

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Sum K-Map:-

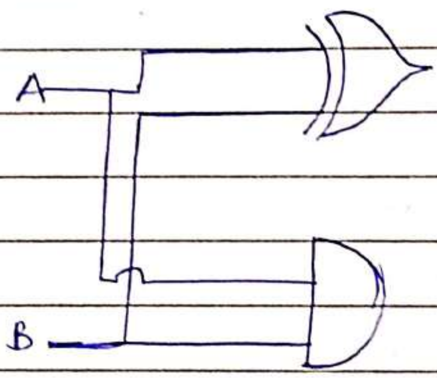
A \ B	0	1
0		1
1	1	

$\bar{A}B + A\bar{B} = A \oplus B$

Carry K-Map:-

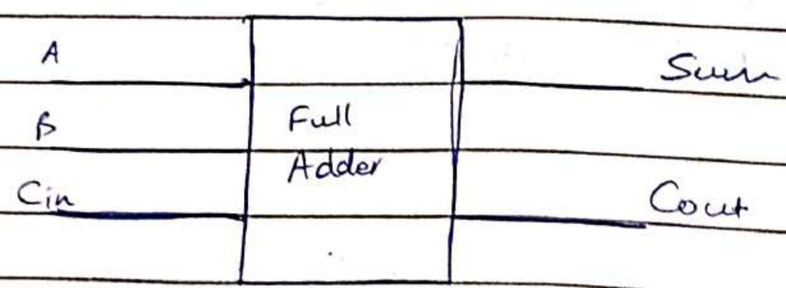
A \ B	0	1
0		
1		1

$AB = A \wedge B$



Full Adder

A type of adder that adds 3 inputs and produc[es] two outputs.



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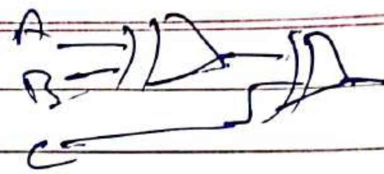


A	B	C_{in}	Sum	C_{out}	
0	0	0	0	0	0
0	0	1	1	0	1
0	1	0	1	0	2
0	1	1	0	1	3
1	0	0	1	0	4
1	0	1	0	1	5
1	1	0	0	1	6
1	1	1	1	1	7

Sum K-Map :-

A \ BC_{in}	00	01	10	11
0	000 (0)	001 1 (1)	010 1 (2)	011 (3)
1	100 1 (4)	101 (5)	110 (6)	111 1 (7)

~~$\bar{A} + A = \oplus A$~~

Carry K-Map :-

A \ BC_{in}	00	01	10	11
0	000 (0)	001 (1)	010 (2)	011 1 (3)
1	100 (4)	101 1 (5)	110 1 (6)	111 1 (7)

~~$\bar{A} B C_{in} + A$~~

$XOR = \bar{A}B + \bar{B}A = A \oplus B$

$XNOR = \bar{A}\bar{B} + AB = \overline{A \oplus B}$

Sum K-Map :-

A \ BC_{in}	00	01	11	10
0	000 (0)	001 1 (1)	011 (3)	010 1 (2)
1	100 1 (4)	101 (5)	111 1 (7)	110 (6)

$A\bar{B}\bar{C}_{in} + \bar{A}\bar{B}C_{in} + ABC_{in} + \bar{A}B\bar{C}_{in}$

~~$\bar{B}\,C_{in}$~~

~~$A\,C_{in}(\bar{B} + B) + \bar{A}C_{in}(\bar{B} + B)$~~

$= C_{in}(A\bar{B} + \bar{A}B) + C_{in}(AB + \bar{A}\bar{B})$

$= C_{in}\ XOR\ (A\ XOR\ B)$

$= A \oplus B \oplus C_{in}$

Carry)

$= C_{in}(A \oplus B) + C_{in}(\overline{A \oplus B})$

$= \bar{C}_{in}X + C_{in}\bar{X}$

$= C_{in} \oplus X$

$= C_{in} \oplus A \oplus B$

C_{out} K-Map:-

A \ BC_{in}	00	01	11	10
0	000 0	001 2	011 1 3	010 2
1	100 4	101 1 5	111 1 7	110 1 6

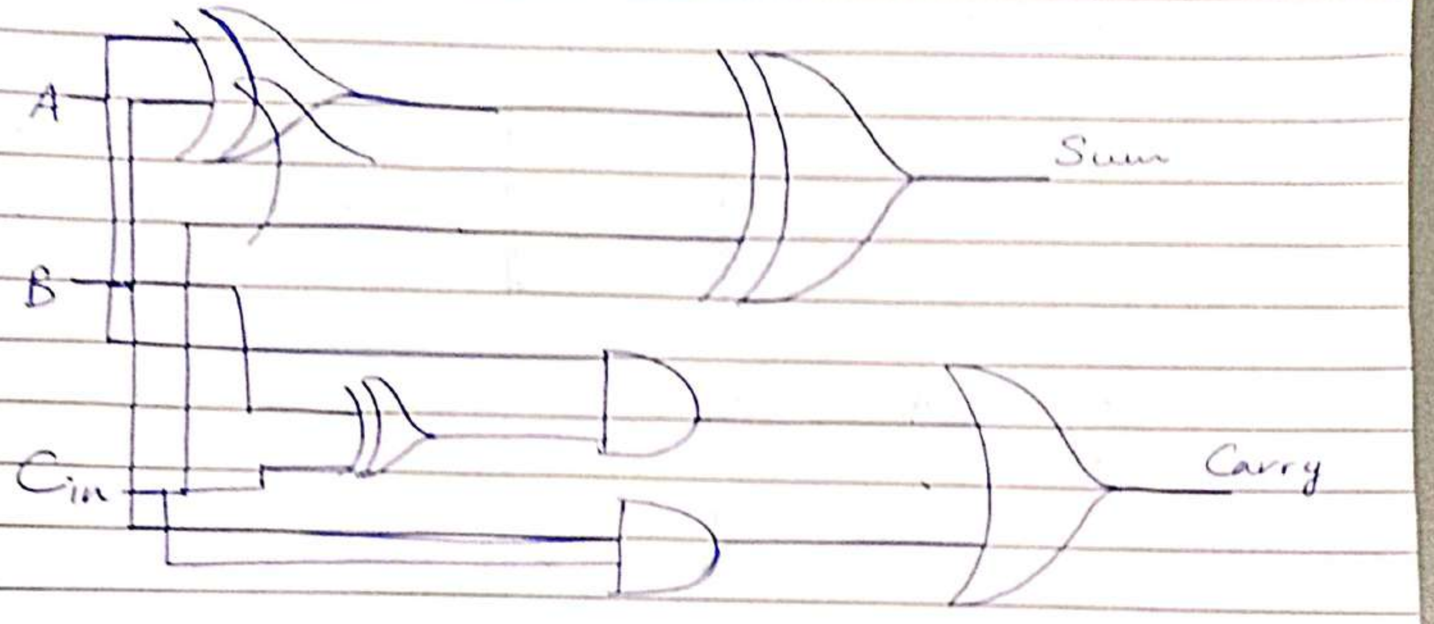
$$A\bar{B}C_{in} + BC_{in} + AB\overline{C_{in}}$$

$$= \cancel{AC_{in}(\bar{B} + B) + BC_{in}} = A(\bar{B}C_{in} + B\overline{C_{in}}) + BC_{in}$$

$$= \cancel{(A+B)C_{in}} = \cancel{A(B\oplus C}$$

$$= A(B\oplus C_{in}) + BC_{in}$$

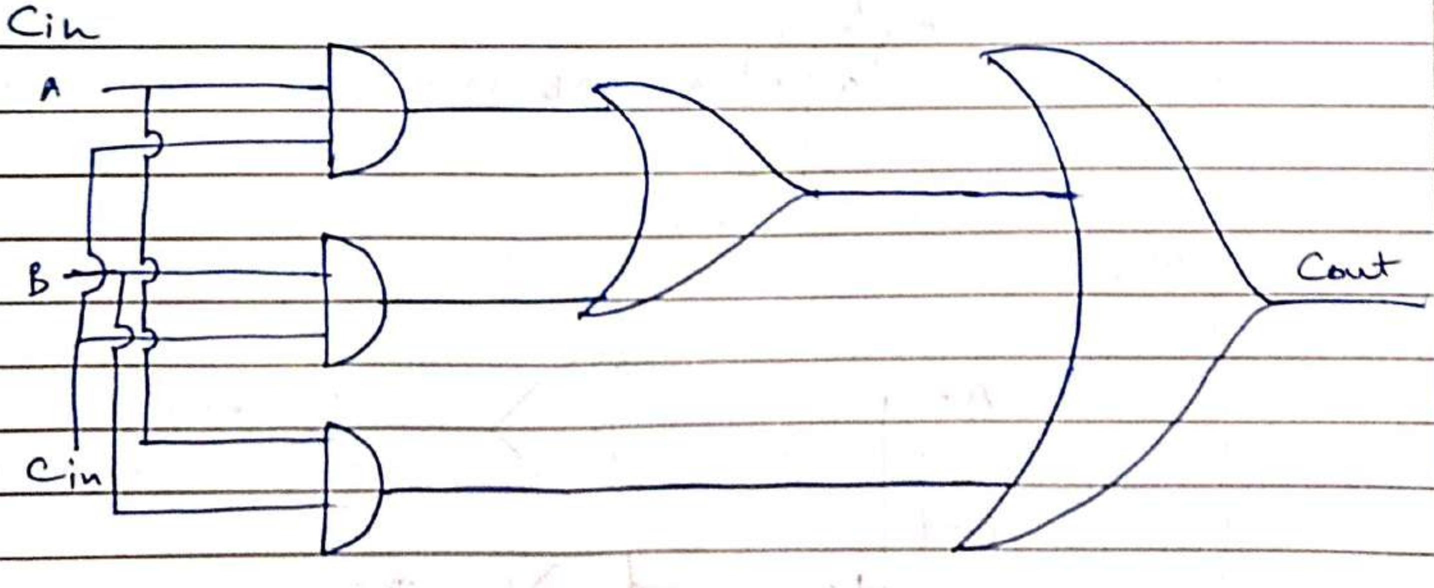
$$F(A,B,C) = B\cdot C_{in} + A\cdot C_{in} + A\cdot B$$



REMEMBER !!!

SOP	POS
A - 1	A - 0
$\bar{A}$ - 0	$\bar{A}$ - 1

- You can't group odd number of outputs in K-maps
- if you grouped $(B + \bar{B})$, don't group anything else.



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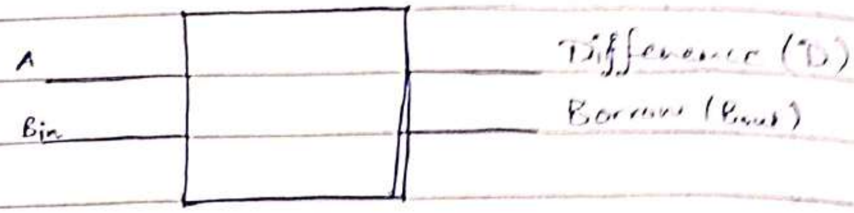
Half Subtractor



A	Bin	D	Bout
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

~~$D = \bar{A}B$~~

K-Map for D:-

A \ Bin	0	1
0	0	1
1	1	0

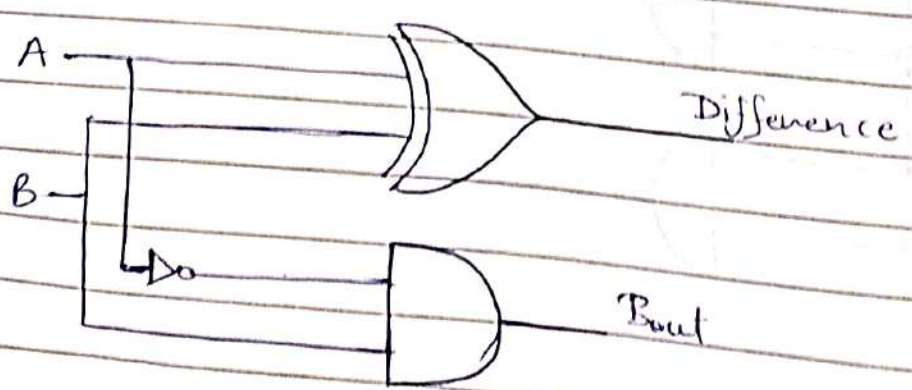
$\rightarrow \bar{A}B + A\bar{B} = A \oplus B$

K-Map for Bout:-

A \ Bout	0	1
0	0	1
1	0	0

$\rightarrow \bar{A}B$

Diagram:



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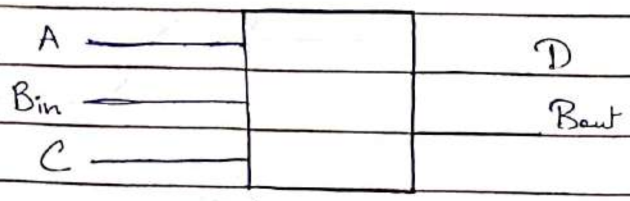
Full Subtractor



A	B_{in}	C	D	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

K-Map for D :-

A \ $B_{in}C$	00	01	11	10
0	0	1	0	1
1	1	0	1	0

$\rightarrow A\overline{B}_{in}\overline{C} + \overline{A}\,\overline{B}_{in}C + AB_{in}C + \overline{A}B_{in}\overline{C}$

$$A\overline{B_{in}}\,\overline{C} + \overline{A}\,\overline{B_{in}}C + AB_{in}C + \overline{A}B_{in}\overline{C} = A(\overline{B_{in}}\,\overline{C} + B_{in}C) + \overline{A}(\overline{B_{in}}C + B_{in}\overline{C})$$

$$= A(\overline{B_{in} \oplus C}) + \overline{A}(B \oplus C)$$

$$= A(\overline{X}) + \overline{A}(X)$$

$$= A \oplus X$$

$$= A \oplus B_{in} \oplus C$$

K-Map for Bout :-

A \ $B_{in}C$	00	01	11	10
0	0	1	1	1
1	0	0	1	0

$\rightarrow \overline{A}C + \overline{A}B_{in} + B_{in}C$

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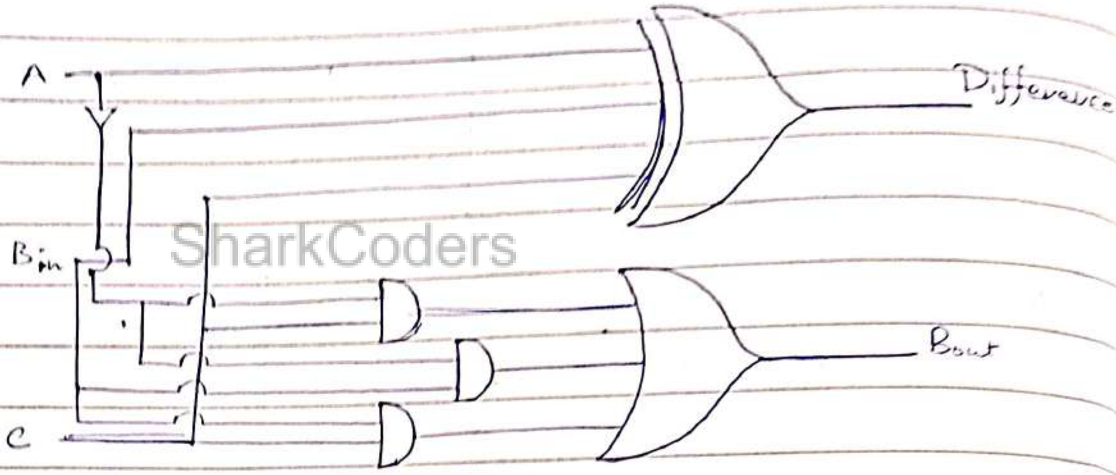
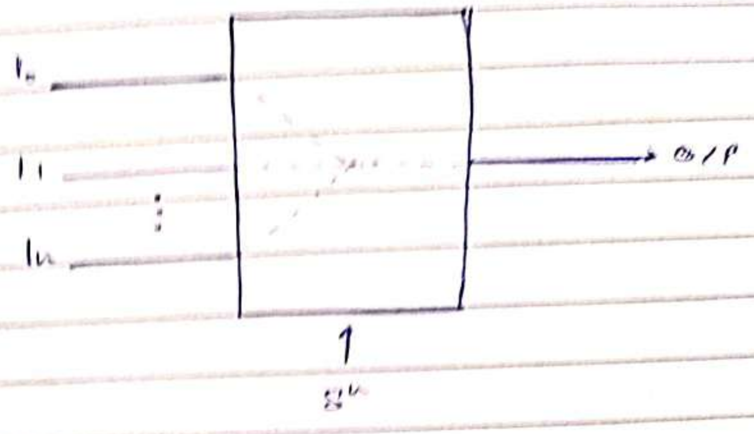
Diagram :-



Multiplexing

8/8/24

Multiplexing



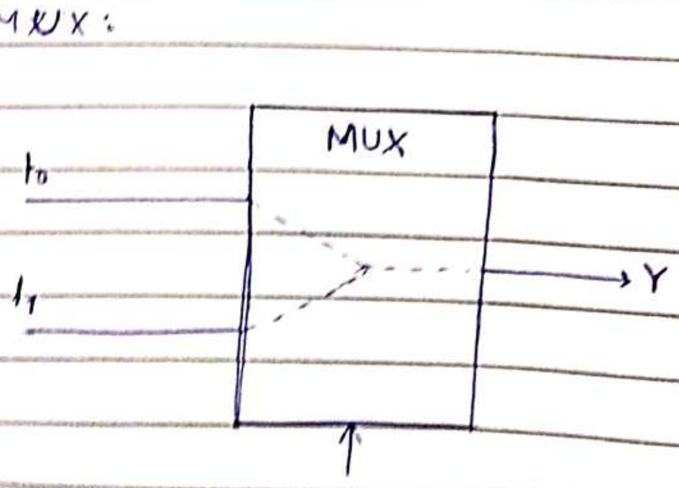
- data selector

- many inputs and one output

MUX

2:1	4:1
→ 4 I/P lines	→ 4 I/P lines
→ 1 select line	→ 2 select lines
→ 1 O/P line	→ 1 O/P line

2:1 MUX:



$S_0 = 0 \rightarrow I_0$
$S_0 = 1 \rightarrow I_1$

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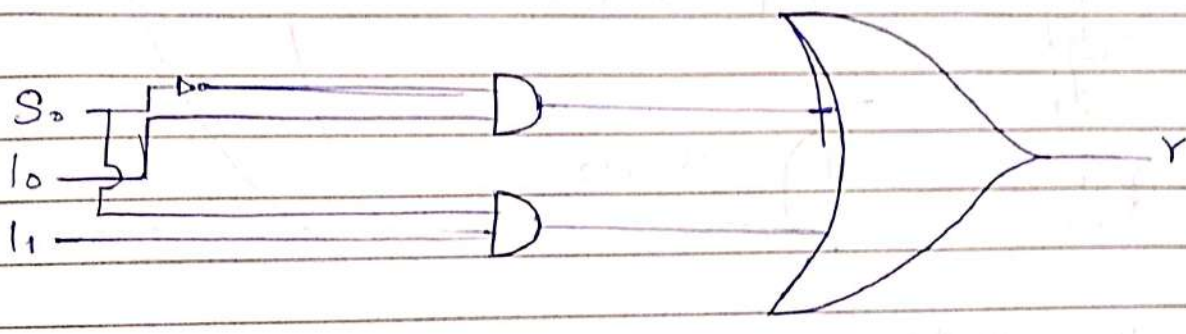
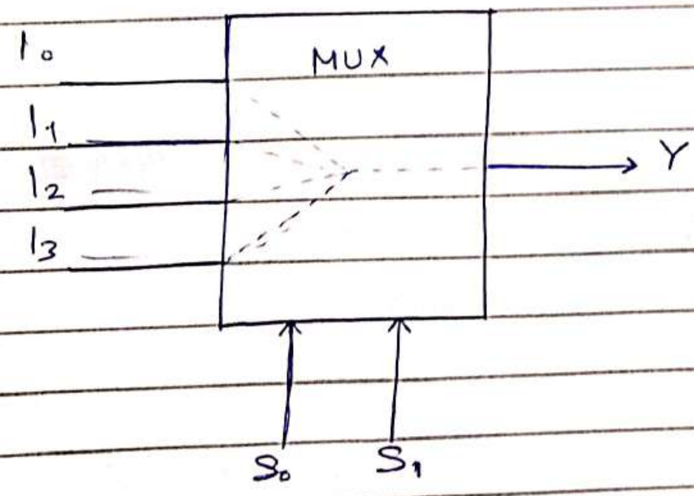
S_0	I_0	I_1	Y
0	0	x	0
0	1	x	1
1	X	0	0
1	X	1	1

$$Y = \bar{S}_0 I_0 + S_0 I_1$$



4:1 MUX



S_0	S_1	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

$$Y = \bar{S}_0 \bar{S}_1 I_0 + \bar{S}_0 S_1 I_1 + S_0 \bar{S}_1 I_2 + S_0 S_1 I_3$$

(NEXT PAGE)

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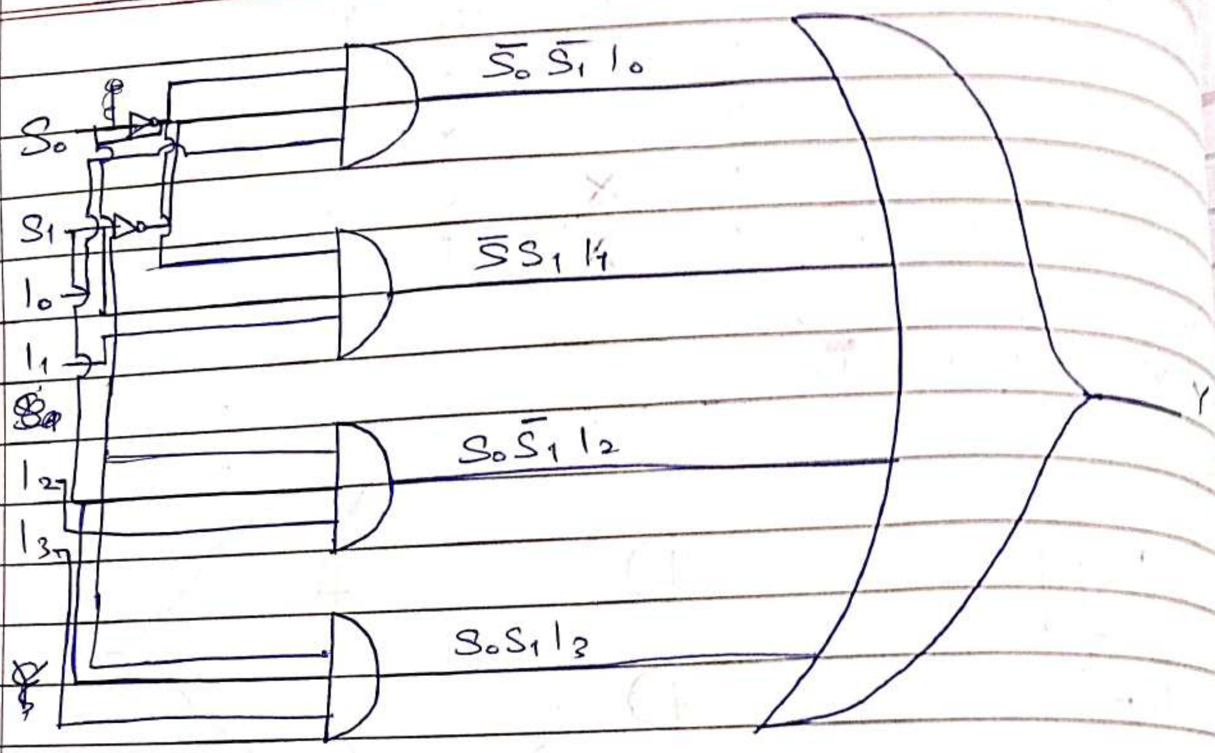


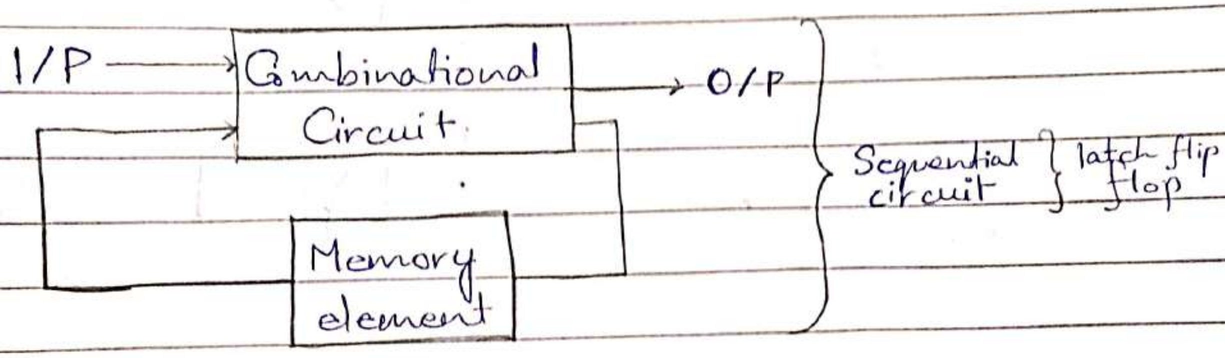
Demultiplexer

- truth tables are opposite outputs.

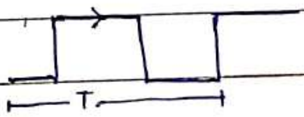
- encoder
- BCD encoder
- Registers and types
- Universal shift register

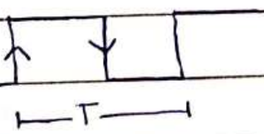
Flip Flops

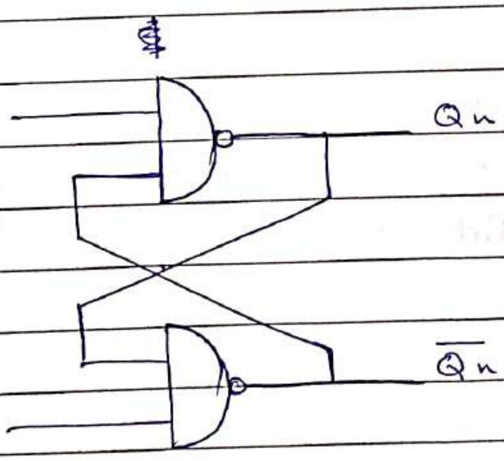
Flip Flops



Latch	Flip-Flops
• no CLK (clock) pulse	CLK (clock) pulse
• level triggered	edge triggered







S	R	Qn
0	0	Invalid
0	1	1
1	0	0
1	1	Hold

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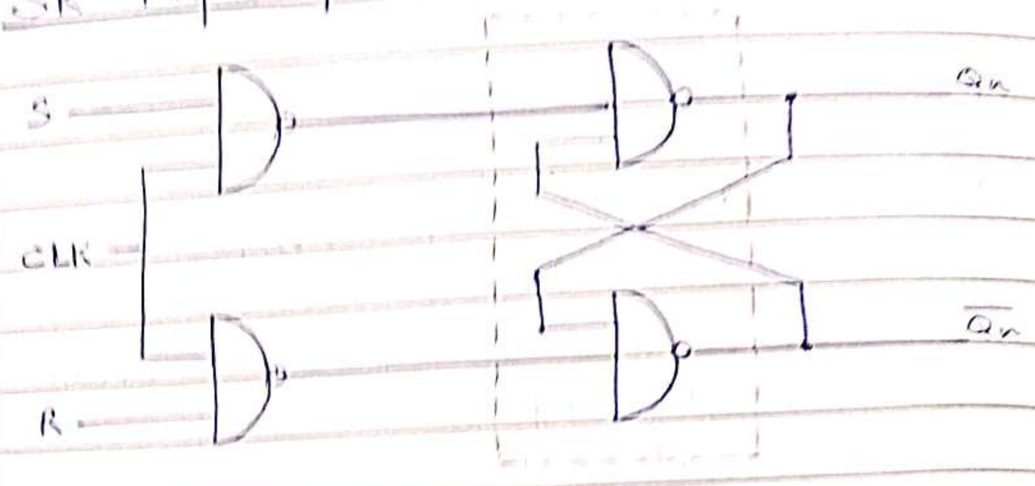
SR Flip Flops



~~CLK~~	S	R	Latch
	0	0	Invalid
	0	1	1
	1	0	0
	1		Hold

CLK	S	R	Q_{n+1}
0	X	X	Q_n
1	0	0	Hold
1	0	1	0 (Reset)
1	1	0	1 (set)
1	1	1	Invalid

BCD to 7 Segments conversion

Comparator:

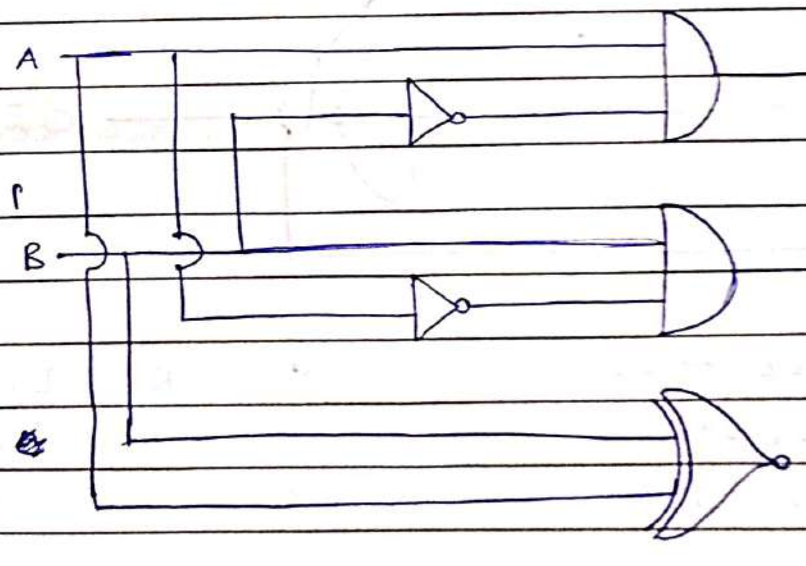
1) Magnitude Comparator

A	B	A>B	A<B	A=B
0	0	0	0	1
0	1	0	1	0
1	0	1	0	0
1	1	0	0	1

$A > B \longrightarrow A\bar{B}$

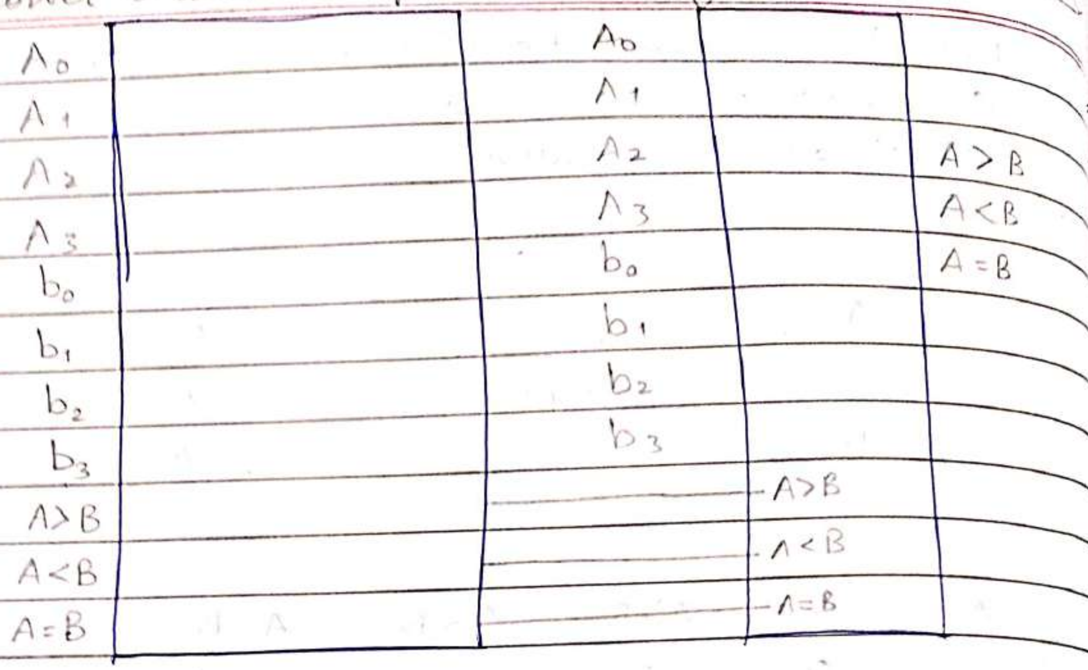
$A < B \longrightarrow \bar{A}B$

$A = B \longrightarrow \bar{A}\bar{B} + AB = A \text{ XNOR } B$

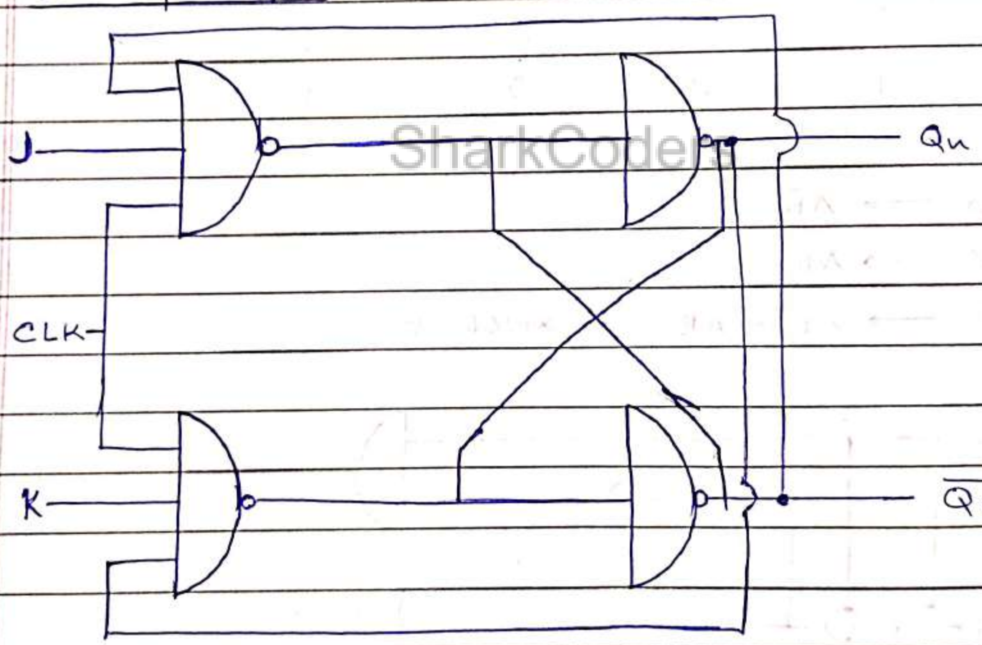


Lower Order Comparator to Higher Order

Cascading Configurator



20/9/24 JK Flip Flops



Case I: $Q_n = 0$, then

$Q_{n+1} = 1$

$\therefore$ It is toggling.

Case II: $Q_n = 1$, then

$Q_{n+1} = 0$

$\therefore$ It is toggling

S	R	Latch
0	0	Invalid
0	1	1
1	0	0
1	1	Hold

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CLK

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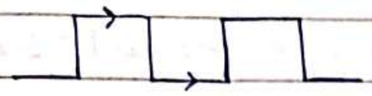
Race Around Condition

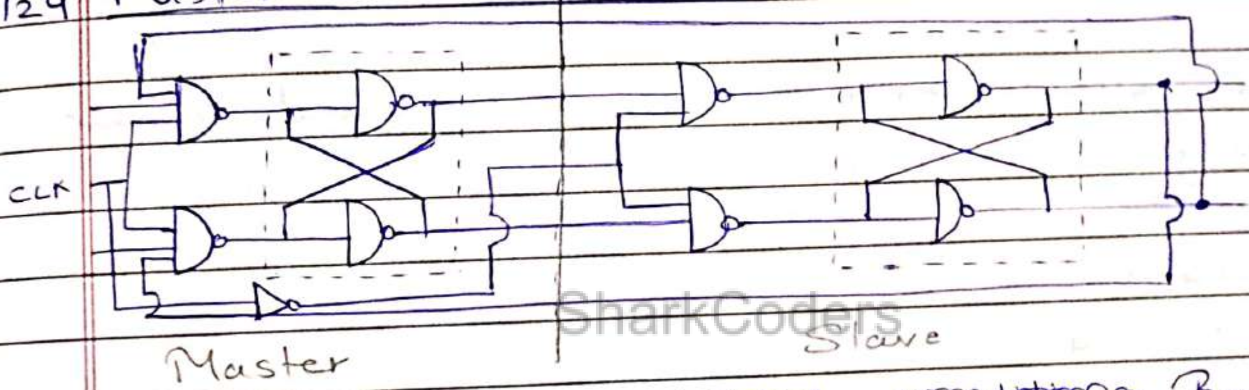
1. Level trigerred JK F.F.

2. When J = K = 1



3. $T_w >>> T_d$ [T_d = propogation delay]
   10ns >> 2ns

1/9/24 ## Master - Slave Flip - Flop



- This solves the Race Around condition and prevents the toggling in output.

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Counters

Device that stores the no. of times a particular event or process has occured, ~~afeten~~ often in relationship to a clock signal.

- counting purpose, count specific event happening in the circuit.

- E.g.: ~~op~~ in UP counter, a counter ~~cou~~ increases count for every rising edge of the clock.

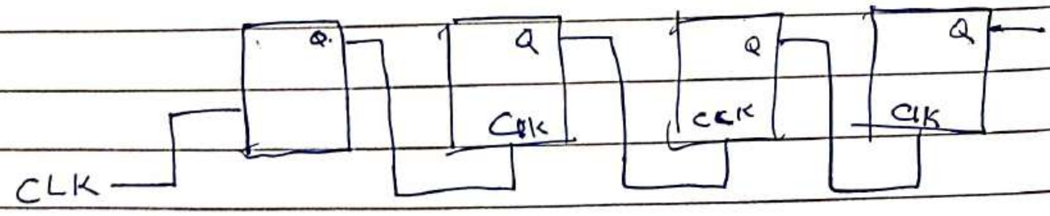
- can follow certain sequence based on our design

- Properties
  - → timing
  - → sequencing
  - → counting

COUNTER
- Asynchronous
- Synchronous

Asynchronous counter

: no uni clock



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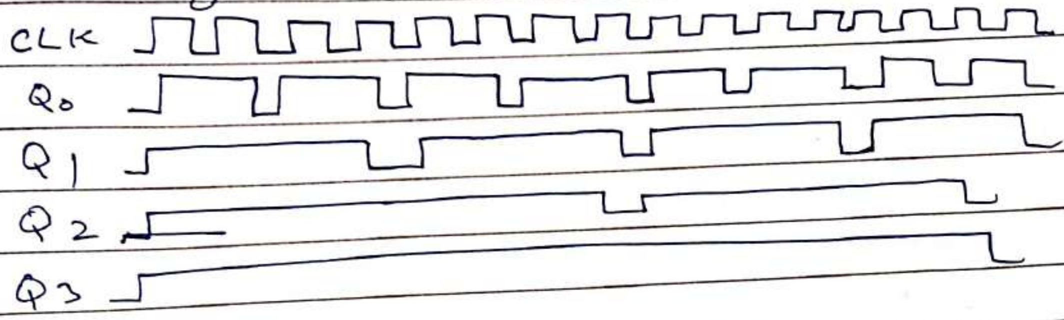
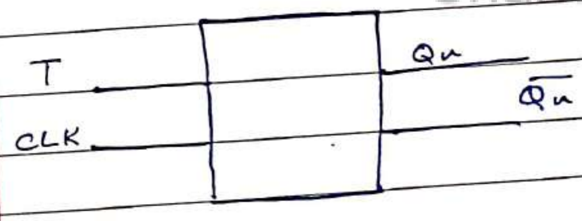
up counter - 1, 2, 3, ... n
down counter - n, n-1, n-2, ... 1

· ripples are generated.



T- Flip Flop

· T- toggle (switching between 0 and 1)



· when T=0, I/P is same as the O/P ($Q_{n+1} = Q_n$)
T=1, O/P is $Q_n = \overline{Q_n}$

T	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

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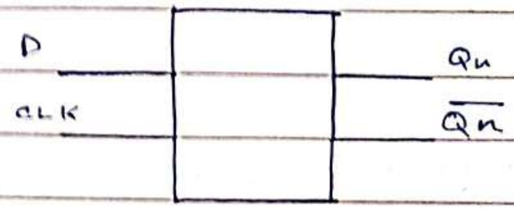
D flip Flop



- when $D = 0$, $O/P = 0$
  $D = 1$, $O/P = 1$

- $Q_{n+1} = D$

-

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

Synchronous Counter

- one global clock which drives each flip flop so O/P changes in parallel.

- advantage: operate on a higher frequency than as it does not have cumulative delay because same clock is given to each flip flop.

- a.k.a. parallel counter.

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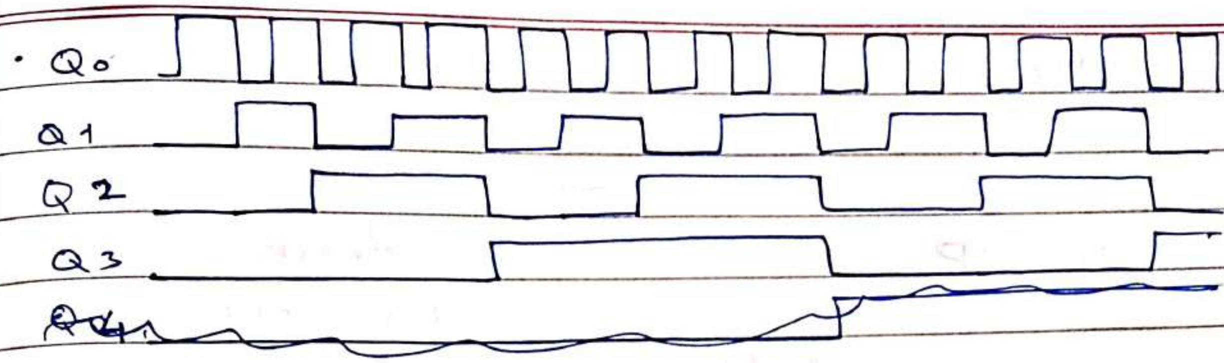

Decade Counter

- counts 10 states then resets to its initial states.
- counts from 0 to 9
- can also go through 0 ~~an~~ to 15. (for 4 bit counter)

CLK Pulse	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	0	0	0	0

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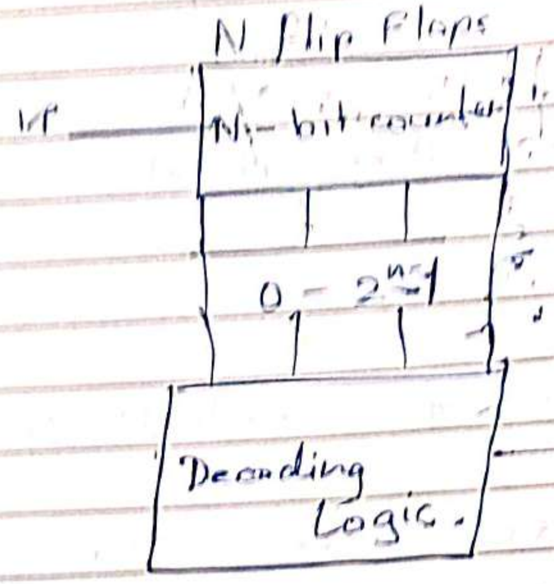
Counter

Binary Counter

- up: 0000 → 1111
- down: 1111 – 0000



→ we can know when counter has reached a certain count

Modulus

The no. of O/P states through which a counter before returning to its first state.

BCD Counter

→ 4 - bit

→ MOD - 10

Applications

- counting
- time measurement
- analog to digital converter

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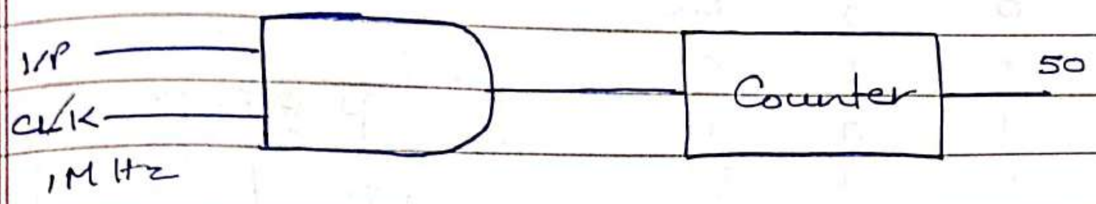
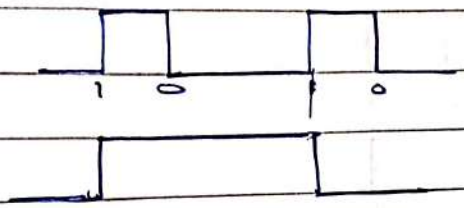
· frequency division



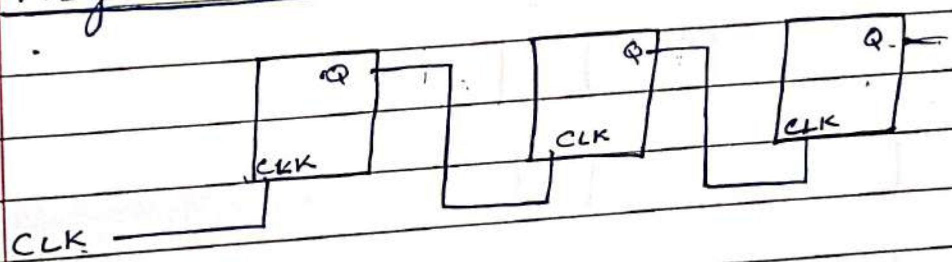


COUNTERS

async (ripple)

sync.

Asynchronous



· easy to design.

· cannot work for high speed operations.

~~Synchronous toggle mode~~

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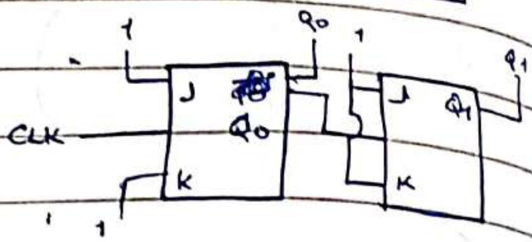
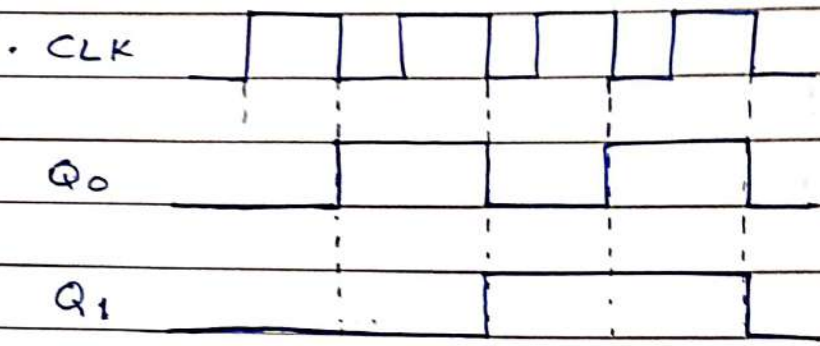
CLK	J	K	Q_{n+1}
↓	0	0	Q_n
↓	0	1	0
↓	1	0	1
↓	1	1	$\overline{Q_n}$

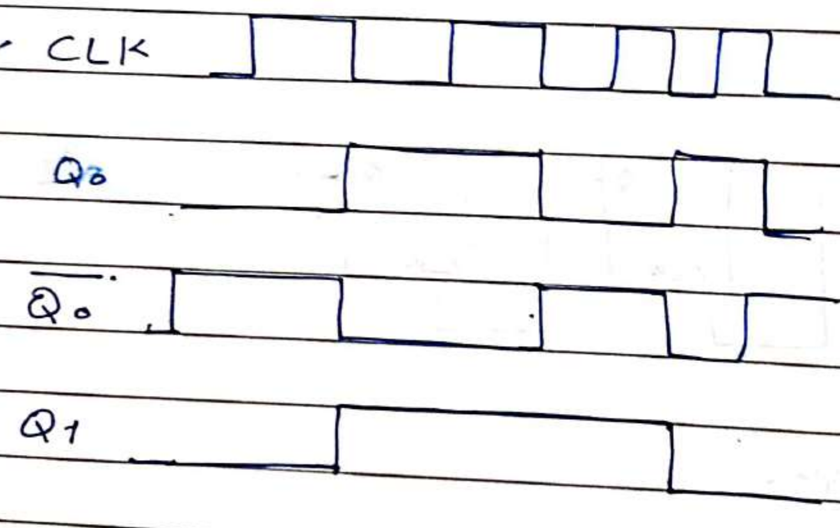
→ 2 bit bin. up.

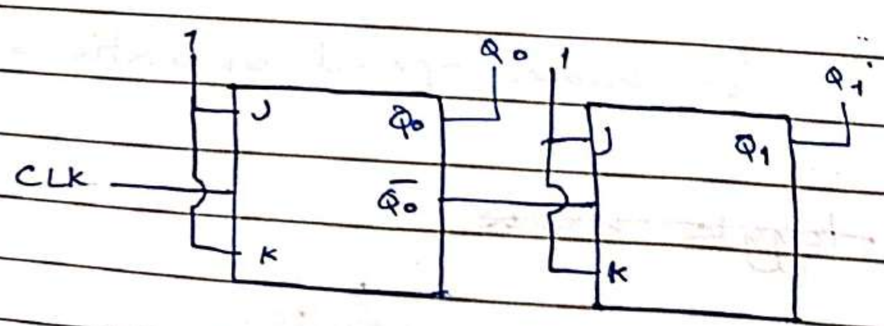




- toggle state at every falling edge

2 bit bin. down





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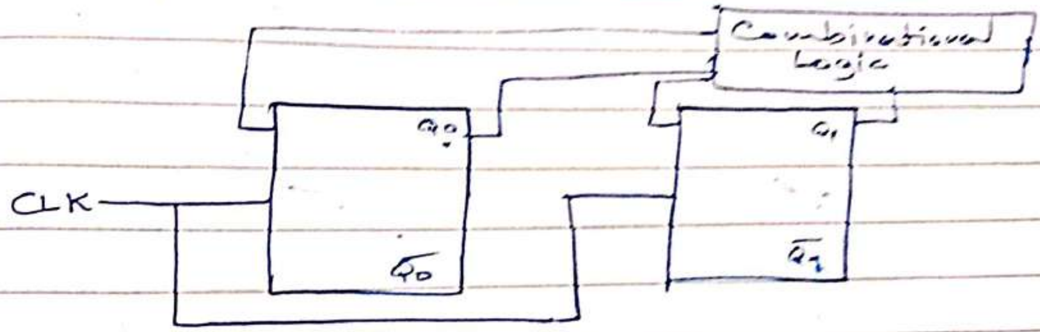
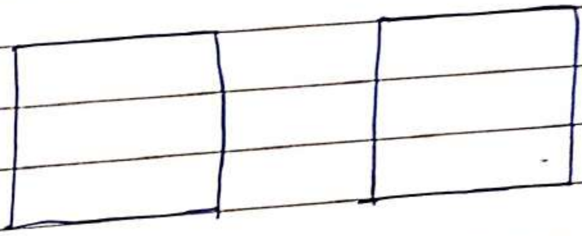
Synchronous

- all flip flops recieve the clk at the same time.



- Steps
  - → find the required no. of flip flops
  - → draw the state diagram
  - → select flip flop and draw excitation table
  - → min. expression of
  - → draw logic circuit



A	B
0	0
0	1
1	0
1	1

Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	x	1
1	0	1	x
1	1	x	0

J	K	Q_n	Q_{n+1}
0	X	0	0
x	1	1	0
1	X	0	1
X	0	1	1

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Present		Next		Required			
Q_0	Q_1	Q_0^+	Q_1	J_1	K_1	J_0	K_0
0	0	0	1	0	x	1	x
0	1	1	0	1	x	x	1
1	0	1	1	x	0	1	x
1	1	0	0	x	1	x	1

Max propagation Delay = $T_{PD} = T_{PD}(FF) + (n-2)\, T_{PD}(AND)$

$$f_{CLK}(max) = \frac{1}{T_{PD}}$$

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Sequential Circuits

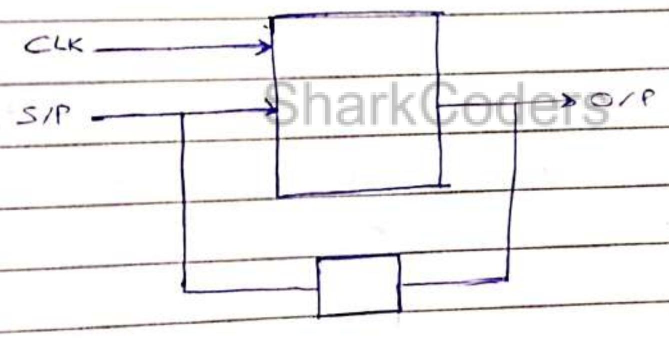
Type of logic circuit whose O/P depends on the present value of its I/P signals but on the past history of its I/Ps.

- has a state

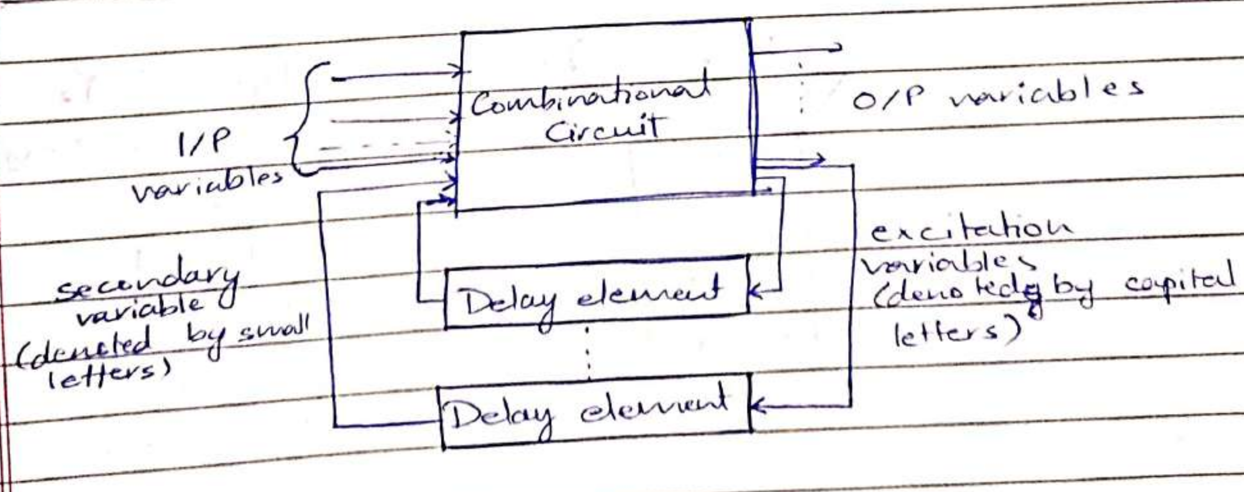
SEQUENTIAL CIRCUIT

Synchronous — Asynchronous

Synchronous S.C.



SA



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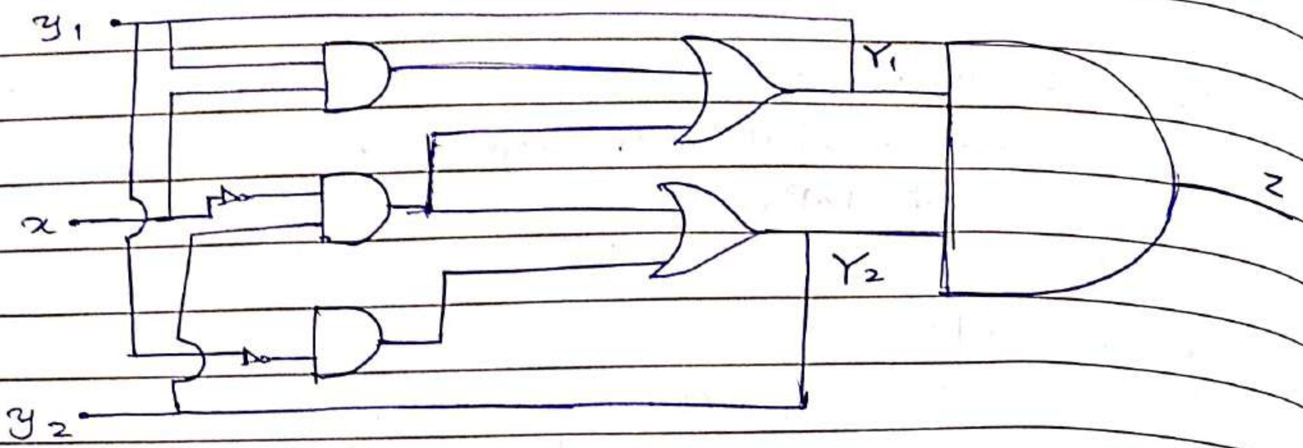

Step I:

$Y_1 = xy_1 + \bar{x}y_2$

$Y_2 = x\bar{y}_1 + \bar{x}y_1$

$Z = Y_1 Y_2 = \bar{x}y_2$

$= Y_1 Y_2$

$= (xy_1 + \bar{x}y_2)(x\bar{y}_1 + \bar{x}y_1)$

$= (xy_1)\cancel{(x\bar{y}_1)} + (xy_1)(\bar{x}y_1) + (\bar{x}y_2)(\bar{x}\bar{y}_1) + (\bar{x}y_2)(\bar{x}$

$= \cancel{xy_1 + x \quad x + y_1 + \bar{x}y_1 + y_2} \quad xy_1 + \bar{x}y_2$

$= \bar{x}y_2 + xy_1 \quad xy_1($

Step II:

$y = xy_1 + \bar{x}y_2$

Map of Y_1

y_1y_2 \ x	0	1
00	0	0
01	1	0
11	1	1
10	0	1

Map of Y_2

$y = x\bar{y}_1 + \bar{x}y_2$

y_1y_2 \ x	0	1
00	0	1
01	1	1
11	1	0
10	0	0

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Step II: Map of Z

$Z = \bar{x} y_2$

$y_1 y_2$ \ x	0	1
00	0	0
01	1	0
11	1	0
10	0	0

Step III: Transition table = combination of all secondary variable

$Y_1 + Y_2 =$

$y_1 y_2$ \ x	0	1
a → 00	00	01
b → 01	11	01
c → 11	11	10
d → 10	00	10

→

a	b
c	b
c	d
a	d

Step IV:

$Y_1 + Y_2 + \ldots \Rightarrow a, b, c, d \Rightarrow [a, z_1], [b, z_2], [c, z_3], [d, z_4]$

a,0	b,0
c,1	b,0
c,1	d,0
a,0	d,0

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Unit IV

Q.1.* Analyze an asynchronous sequential circuit with two ~~exie~~ excitation func^{n}s with two feedback lo.. given as:

$Y_1 = xy_1 + \bar{x}y_2$

$Y_2 = x\bar{y}_1 + \bar{x}y_2$

a) Draw the logic diagram of the circuit

b) Derive the transition table and obtain the flow table (10)

Q 2. An asynchronous sequential circuit is described by the following excitation and O/P func^n,

$Y = x_1x_2 + y(x_1 + x_2).$

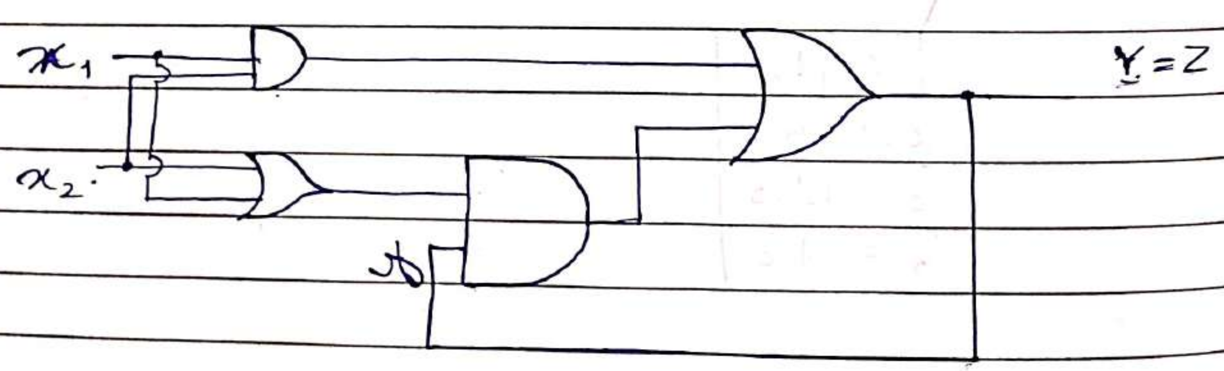
$Z = Y$

a) Draw the logic diagram of the circuit

b) Derive the transition table, flow table and O/P map.

c) Describe the behaviour of the circuit.

Ans. a) The logic diagram



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b) The truth table

y	x_1	x_2	x_1x_2	$y(x_1+x_2)$	Y	Z
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	1	1	1	0	1	1
1	0	0	0	0	0	0
1	0	1	0	1	1	1
1	1	0	0	1	1	1
1	1	1	1	1	1	1

$y \backslash x_1x_2$	00	01	11	10
0	0	0	1	0
1	0	1	1	1